Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1.-6. (canceled)

7. (currently amended) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

~~pattering~~ patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged in a stagger manner so that side edges of the adjacent hole patterns are only partially opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film,

wherein the length of a portion where the opposing capacitors are overlapped in the mask layout is set so that the value of the parasitic capacitance between adjacent cell capacitors is not more than 10% of the set cell capacitance value.

8. (original) The method according to claim 7, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

9-15. (cancelled)

16. (previously presented) The method according to claim 7, wherein a relative dielectric constant of the interlayer insulating film is 3.5 or less.

17. (previously presented) The method according to claim 7, wherein the interlayer insulating film is made of silicon oxide including fluorine.

18-21. (canceled)